[Total No. of Questions -9] [Total No. of Printed Pages :4]
(2127)

5503

B.Tech. 3rd Semester Examination

Data Structure and Algorithms (CSE)

Paper - IT (ID) 3003

Time Allowed : 3 Hours **Maximum Marks : 100**

The candidates shall limit their answers precisely with the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Candidates are required to attempt five questions in all selecting at least one question from each section A, B, C and Section D. Entire Section E is compulsory.

SECTION - A

1. Discuss in brief the uses of data structures. Differentiate between linear and non-linear data structures. Discuss in brief the concept of algorithmic complexity and time space trade off. **(15)**

2. Define a linked list. How a linear linked list is different from doubly linked list. Write an algorithm to insert and delete a node in a doubly linked list. **(15)**

SECTION - B

3. (a) Discuss various tree traversals in detail giving suitable examples. **(08)**

(b) Write an algorithm to insert an element in a binary search tree **(07)**

4. What is binary search tree? How it is different from binary tree? Write an algorithm to delete a node from a binary search tree. **(15)**

SECTION - C

5. What do you mean by a graph? Discuss various methods of representing the graph in memory giving merits and demerits of each method. **(15)**

6. Write short note on the following

(a) Simple graph **(04)**

(b) Multi graph **(04)**

(c) Acyclic Graph **(04)**

(d) Connected graph **(03)**

SECTION - D

7. Explain the procedure of merge sort giving suitable example. **(15)**

8. Explain the linear search in detail. List down the conditions where linear search is preferred over binary search. **(15)**

SECTION - E

9. (a) Give the advantages of linked list. **(04)**

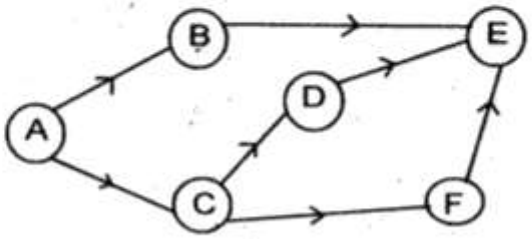
(b) How a linked list is represented in memory? **(04)**

(c) Define the weigh of a tree and give an example. **(04)**

(d) Differentiate between graph and a tree. **(04)**

(e) What do you mean by hashing? Discuss in brief. **(04)**

(f) Give the BFS and DFS of the follwoing graph. **(04)**



(g) Discuss various applications of graph in brief. **(04)**

(h) Compare selection sort with bubble sort. **(04)**

(i) Which data structure is best suited for the insertion sort and why? **(04)**

(j) How a tree is represented in memory? **(04)**

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Total No. of Questions - 9] Total Pages : 3

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5922

B.Tech. IIIrd Semester Examination

DATA STRUCTURE AND ALGORITHM

(CSE/IT)

Paper : IT(ID) – 3003

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *five* questions in all, selecting *one* each from Sections A, B, C and D. Section E is compulsory.

SECTION–A

1. What are the various measures of complexity of an algorithm ? Discuss each of them with example. 15

2. What is a Doubly link list ? Write algorithm for each of the operation possible on Doubly link list. 15

SECTION–B

3. Giving a Binary tree T, write algorithm to

(a) count the number of Non-leaf elements of T.

(b) check if the tree is balanced. 15

4. What is a Binary search tree ? Write the operation of insertion and deletion in a Binary search tree. 15

SECTION–C

5. What are the various techniques for representation of graph ? Explain each of them with example. 15

6. Explain the Dijkstra's algorithm to find the shortest distance in a weighted graph. 15

SECTION–D

7. Explain the following searching algorithm with their complexity :

(a) Binary search.

(b) Linear search. 15

8. Give an array :

17 8 2 3 6 12 14 1 15

How these will be sorted in the following :

(a) Radix sort.

(b) Selection sort.

(c) Bubble sort. 15

SECTION–E

9. Attempt all the following :

(a) What is the complexity of Insertion sort ?

(b) What is a Data structure ?

(c) Convert a ^ b ^ c + d * e – f into postfix expression.

(d) Define Heap.

(e) What is a Circular link list ?

(f) What is a B-tree ?

(g) What is a Height balanced tree ?

(h) What is an AYL tree ?

(i) How a node is represented in C ?

(j) How an element is searched in singly link list ?

4×10=40

Total No. of Questions – 9] Total Pages : 3

(2119)

5132

B.Tech. IIIrd Semester Examination

DATA STRUCTURE AND ALGORITHM

(CSE/IT)

Paper : IT(ID) – 3003

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *five* questions in all, selecting at least *one* question each from Section A, B, C & D. Section E is compulsory.

SECTION–A

1. What is Complexity of an algorithm ? How is it measured ? Discuss Time space trade off with an example. 20

2. Write an algorithm to insert an element in two-way link list. 20

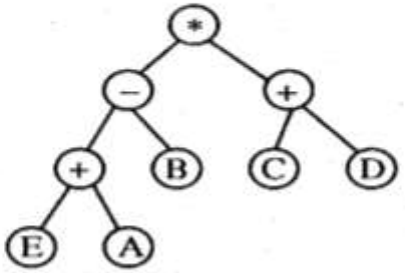
SECTION–B

3. (a) Build a heap tree from following list of numbers : 44, 30, 50, 22, 60, 55, 77 and 55. 15

(b) What is AVL tree ? 5

4. (a) Write an algorithm for INORDER traversal of a binary tree. 14

(b) Traverse the given tree in Preorder, Inorder and Post-order 6



SECTION–C

5. Write Dijkstra's algorithm for shortest path. 20

6. What do you mean by Adjacency mátrix ? Give an example and explain how it is used in graphs. 20

SECTION–D

7. Write an algorithm for insertion sort and explain it with an example. 20

8. Assume we have a sorted array of elements in descending order. Can binary search algorithm still be implemented on it ? If yes, write the modified algorithm. If not justify. 20

SECTION–E

9. Write short answers of the following :

(a) Give applications of Linked list.

(b) What is height of a tree ?

(c) What is Complete binary tree ?

(d) Differentiate between Graph and Tree.

(e) Give complexity of Selection sort and Bubble sort.

(f) What is Hash table ?

(g) What is Collision ?

(h) Convert A*(B + D)/E – F*(G + H/K) into Post-fix expression.

(i) Differentiate between Binary search and Linear search.

(j) What is Big O notation ?

2×10=20

(2115) Total Pages : 3

5885

B. Tech. 3rd Semester Examination

DIGITAL ELECTRONICS

Paper–EC-ID 3001

(EE/ECE/CSE/IT)

(New Syllabus)

Time : Three Hours

Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : *Attempt* ***one*** *question each from* **Sections–A, B, C** *and* **D** *and* ***entire*** **Section–E.**

Section–A

1. Fill in the blanks (?)

Binary	Octal	BCD	Hexadecimal
11110101	365?	?	?
?	4567	?	?
?	?	3456	?
?	?	?	9abc

20

2. (a) What is error detection and correction code Hamming code ? Explain with the help of an example. 8

(b) Perform following subtraction using 2's Complement method :

(i) 11111100-01010100

(ii) 11110001-10001111 . 6

(c) Perform following subtraction using 10's Complement method :

(i) 97-45

(ii) 44-87 6

Section–B

3. Minimize the following Boolean expression using quine Mccluskey procedure

$f(v, w, x, y, z) = \Sigma(0, 14, 5, 7, 8, 9, 13, 15, 17, 19, 21) + \Sigma dc(12, 14, 23)$.

Verify the result using K map. 20

4. Write down the truth table of a full adder circuit and realize it using (i) 9 Nand gate (ii) 8 : 1 Multiplexer (iii) 4 : 1 Multiplexer. 20

Section–C

5. Draw the diagram of DCTLd gate and explain its operation. Why Base current hogging is there ? 20

6. Draw the Diagram of an Ex = or gate using MOS gates. 20

Section–D

7. Write down the truth table of all flip-flops. Draw the diagram of j-k flip-flop and explain its operation. 20

8. (a) Draw the diagram of any A-D Convertor and explain its operation. 10

(b) Draw the diagram of shift register and explain its operation as SISO, PISO, PIPO, SIPO. 10

Section–E

9. (a) What is a positive logic and negative logic ? 2

(b) Draw the truth table of all logic gates. 2

(c) Realize an AND gate using NOR gates only. 2

(d) What is the difference between multiplexer and demultiplexer ? 2

(e) Give comparison between various A-D converters ? 2

(f) What is the difference between ROM and RAM ? 2

(g) How Race around condition is eliminated in Master-slave J-k flip-flop ? 2

(h) Perform following binary subtraction :
0101010-11010101 2

(i) Convert following binary number into gray code and vice-versa :
10101111 2

(j) Define Multiplexer and Demultiplexer. 2

Total No. of Questions - 9] [Total No. of Printed Pages: 3
(2116)

5066

B.Tech. 3rd Semester Examination

DIGITAL ELECTRONICS (EE/ECE/CSE/IT)

Paper - EC (ID) 3001

Time Allowed : 3 Hours *Maximum Marks : 100*

Note:- The candidates shall limit their answers precisely with the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Attempt one question from each section and entire section E.

SECTION - A

1. Fill in the blanks shown with? 15

Binary	Octal	Decimal	Hexadecimal
1011 1101	?	?	?
?	7654321	?	?
?	?	123456	?
?	?	?	1234

2. (a) What are various error-correcting codes? Discuss them briefly.

   (b) Perform BCD addition (I) 65 + 78

   (c) Perform BCD Subtraction 78-76 15

SECTION - B

3. What do you understand by K-Map? Minimize the following Boolean expression using K-Map : $F(w, x, y, z) = \Sigma (0, 1, 4, 5, 7, 8, 9, 13, 15) + \Sigma dc (12, 14)$. Verify your result using Quine Mccluskey procedure.

4. Write down the truth table of full subtarctor and realize it through N and gates only. 15

SECTION - C

5. What is CMOS gate? Explain its operation. Draw an x-or gate using MOS gates. 15

6. Draw the diagram of an ECL gate and explain its operation. 15

SECTION - D

7. Draw a diagram Write down truth table of various flip-flops. What is a Race around condition? How it is eliminated in Master Slave J-K Flip-flop? Draw its diagram. 15

8. (a) Draw the diagram 555 timer and explain its operation in an astable mode. 8

   (b) Draw the diagram of an A-D convertor and explain its operation. 7

SECTION - E

9. (a) Convert the following numbers to hexadecimal number and vice versa : (i) 11111010 (ii) 11101000 4

(b) Why 2's complement is used in computers for representation of negative numbers? 4

(c) Realize an And gate using NOR gates only. 4

(d) Differentiate between combinational circuit and sequential circuit? 4

(e) State various postulates and theorems of Boolean algebra 4

(f) Differentiate between minterm and maxterm. 4

(g) Perform following binary subtraction : 11111111-11010101 4

(h) What do you mean by an error? 4

(i) List the steps in designing a synchronous counter 4

(j) Write down truth table for EX-OR gate. 4

[Total No. of Questions -9] [Total No. of Printed Pages :4]
(2127)

5495-A

B.Tech. 3rd Semester Examination

Digital Electronics (EE/ECE/CSE/IT)

Paper - EC(ID) - 3001

Time Allowed : 3 Hours **Maximum Marks : 100**

The candidates shall limit their answers precisely with the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt **One** question from section A, B, C, D & entire E section.

SECTION - A

I. (A) Convert decimal number (39.12) in binary form?

(B) Multiply $(10.1)_2$ & $(1.01)_2$ & convert the result into equivalent decimal number.

(C) Divide $(1EC\ 87)_{16}$ by $(A5)_{16}$. **(15)**

II. Write short note on.

(A) Floating point representation & its significance?

(B) Error detection code & its features?

(C) Error carrection code & its features? **(15)**

SECTION - B

III. Simplify the following expression & realise using Basic gates.

(A) $XY+\overline{XZ}+X\overline{YZ}(XY+Z)$

(B) $\overline{\overline{AB}+\overline{A}+AB}$

(C) $\overline{AB}+\overline{\overline{AB}}$ **(15)**

IV. Simplify using K-map & draw NAND ckt for simplified expressions.

(A) $Y=\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}+\overline{A}\,\overline{B}C\,\overline{D}+A\overline{B}\,\overline{C}\,\overline{D}+\overline{A}\,CD+A\,\overline{B}C\,\overline{D}$

(B) Reduce & find simplified SOP form

$y=\pi M\,(0,1,2,3,4,6,10,11,13)$ **(15)**

SECTION - C

V. Design & Explain working of

(A) CMOS INVERTOR circuit

(B) CMOS NAND gate **(15)**

VI. Write the specification & charactristics of digital IC's? **(15)**

SECTION - D

VII. Design & draw 3 bit Gray code Synchronous counter? **(15)**

VIII. (A) Explain working of 555 timer as Astable multivibrator. **(9)**

(B) Find duty cycle & frequency of Astable multivibrator using 555 timer if

$C = 0.001\mu F$, $RA = 2.2K\Omega$, $R_B = 90K\Omega$ **(6)**

SECTION - E

IX. (a) What is a universal shift register ? Explain

(b) A certain memory stores 8K x 16 bit words. How many data input lines, data output lines & address lines does it have? What is its capacity in bytes?

(c) Prove that $\overline{ABC}\ \overline{(A+B+C)} = \bar{A}\,\bar{B}\,\bar{C}$.

(d) How do open collector output differs from Totem poll output?

(e) What is Inhibit gate. Realise Inhibit gate using NAND, NOR gates.

(f) Make comparison between DTL & TTL logic families?

(g) What are the shortcoming of J-K flipflop & how it can be removed?

(h) An astable multivibrator uses 555 timer. It is required that duty cycle is 0.5 & frequency = 10KHz & $C = 0.001\mu f$. Calculate R_A & R_B ?

(i) Write the design procedure steps for the design at synchronous counter?

(j) Explain the diffrence between Minterm & Maxterm?

(4X10=40)

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Total No. of Questions - 9] Total Pages : 3
(2118)

5914

B.Tech. IIIrd Semester Examination

DIGITAL ELECTRONICS (EE/ECE/CSE/IT/EEE)
Paper – EC(ID)–3001

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *one* question from each Section A, B, C & D and the entire Section E.

SECTION–A

1. Fill in the blanks shown with ?

Binary	*Octal*	*Decimal*	*Hexadecimal*
1011 1101	?	?	?
?	7654321	?	?
?	?	123456	?
?	?	?	1234

15

2. (a) What is Hamming code ? Discuss.
(b) Perform Binary addition : 1010111 + 1111000.
(c) Perform Binary Subtraction : 11111111 – 10101010.
15

SECTION–B

3. Simplify following Boolean function using quine Mccluskey procedure :

$F(w, x, y, z) = \Sigma(2, 3, 6, 7, 8, 9, 12, 13 + \Sigma dc\ (14, 15)$.

Verify your result using K Map. 15

4. Write down the truth table of Full adder, realize it through
(i) Nand gates only.
(ii) Nor gates. 15

SECTION–C

5. Explain the operation of a CMOS gate. Draw a half adder circuit using MOS gates. 15

6. Draw the diagram of a TTL gate and explain its operation. 15

SECTION–D

7. Draw a diagram. Write down truth table of various flip-flops. What is a Race around condition ? How is it eliminated in Master Salve J-K flip-flop ? Draw its diagram. 15

8. What is a Shift Register ? Explain its operation as SISI, PISO, SIPO, PIPO, Ring counter and Twisted ring counter. 15

SECTION–E

9. Write short answers :

(a) What is a Positive logic and Negative logic ?

(b) Draw the truth table of all logic gates.

(c) Realize an AND gate using NOR gates only.

(d) Give comparison between various A–D converters.

(e) What is Base current Hogging ? How is it eliminated ?

(f) What is a Register ? List various methods of loading the data into shift register.

(g) What is the difference between ROM and RAM ?

(h) How Race around condition is eliminated in Master-slave J-K flip-flop ?

(i) Perform following binary subtraction :

0101010 – 11010101

(j) Convert following Binary number into Gray code and vice-versa : – 10101111. .

4×10=40

Total No. of Questions - 9] Total Pages : 3

(2119)

5124

B.Tech. IIIrd Semester Examination

DIGITAL ELECTRONICS (EE/ECE/CSE/IT/EEE)

Paper : EC(ID)–3001

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *one* question each from Sections A, B, C and D, and the entire Section E.

SECTION–A

1. Write short notes on the following :

(a) Error detection code.

(b) Error correction code.

(c) ASCII code. 5×3=15

2. (a) Solve $(100.1001)_2 \times (0.01011)_2$.

(b) Convert Binary $(1001011)_2$ and $(111101)_2$ to Gray code.

(c) What is the weight of MSB in 16-bit computer and 8-bit computer ?

(d) Solve $(57)_{10} - (32)_{10}$ using 2's complement method.

(e) Describe the 9's and 10's complement methods. 3×5=15

SECTION–B

3. Write the truth table of Full Adder circuit and realise the expression with NOR gate. 15

4. Discuss the procedure to use K-map for simplification of 6 variables in SOP form and simplify the variables using K-map for the function

$f(A, B, C, D, E, F) = \Sigma$ (0, 1, 2, 3, 16, 17, 18, 19, 32, 33, 34, 35, 48, 49, 50, 51, 60, 61, 62, 63) 15

SECTION–C

5. Explain the comparisons of Digital IC logic family. 15

6. What are the advantages of ECL ? Explain how ECL gate works. 15

SECTION–D

7. Explain the operation of Dual slope A/D converter in detail. Also detail the performance characteristics of A/D converter. 15

8. Design a mod-8 synchronous μP counter using T flip-flop. 15

SECTION–E

9. Write short answers of the following :

(a) What are the advantages of Gray code over Binary ?

(b) Why is a code necessary ? Discuss.

(c) Specify the applications of SSI, LSI, MSI, VLSI and ULSI.

(d) Draw CMOS, NOR circuit with its working.

(e) What is the difference between Current sourcing and Current sinking ?

(f) Explain the difference between Combinational and Sequential circuits.

(g) What are the differences between Decoder/Encoder, Mux/Demux ?

(h) Realise a 4×1 multiplexer for the function

$$F = \sum m\ (0, 3, 4, 7).$$

(i) Which is the fastest ADC, and why ?

(j) Realise AND, OR, NOT operating performance using NAND gates. 4×10=40

Total No. of Questions - 9] [Total No. of Printed Pages: 4
(2116)

5072

B.Tech. 3rd Semester Examination

COMPUTER ORGANIZATION (CSE / IT)

Paper - IT (ID) 3001

Time Allowed : 3 Hours ***Maximum Marks : 100***

Note:- *The candidates shall limit their answers precisely with the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.*

Attempt five questions in all selecting at least one question from section A,B,C & D. Section E is compulsory.

SECTION - A

1. (a) Explain the generations of computers. (8)

(b) Draw the logic diagram of a 2-to-4 line decoder with only NOR gates. Include an enable input. (7)

2. What is the difference between serial & parallel transfer? Using a shift register with parallel load, explain how to convert serial input data to parallel output & parallel input data to serial output. 15

SECTION - B

3. Explain Booth's algorithm for multiplication by taking a suitable example. 15

4. (a) Explain the difference between hardwired & microprogrammed control. Is it possible to have a hardwired control associated with a control memory? (6)

(b) Define the following : (i) Micro operation (ii) Micro instruction (iii) Micro program (3x3=9)

SECTION - C

5. (a) How many times does the control unit refer to memory when it fetches an executes and indirect addressing mode instruction if the instruction is (i) a computational type requiring an operand from memory (ii) a Branch type. (8)

(b) What must the address field of an indexed addressing mode instruction be to make it the same as a register indirect mode instruction? Explain. (7)

6. Explain instruction pipelining, its possible conflicts & how you remove them? 15

SECTION - D

7. (a) What is difference between isolated I/O & memory - mapped I/O? What are the advantage & disadvantage of each? 10

(b) Why does DMA have priority over the CPU when both request a memory transfer? 5

8. (a) The access time of a cache memory is 100ns and that of main memory 1000ns. It is estimated that 80% of the memory requests are for read & remaining 20% for write. The hit ratio of read accesses is 0.9. A write - through procedure is used.

(i) What is the average access time of the system considering only memory read cycles?

(ii) What is the average access time of the system for both read & write requests?

(iii) What is the hit ratio taking into consideration the write cycles? 10

(b) A two - way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128k x 32. What is the size of the cache memory? Explain. 5

SECTION - E

9. (a) Simplify the boolean function $F(A, B, C) = \Sigma (0, 2, 3, 4, 6)$ using K-map. 4

(b) Draw a space - time diagram for a six segment pipe line showing the time it takes to process eight tasks. 4

(c) What is the use of control memory? 2

(d) What is speed up factor in pipeline computers? 2

(e) Define 10P?

(f) Define Cache Through in Cache 2

(g) What is address space & memory space? 2

(h) What is page fault? 2

(i) Explain the following in 3-4 lines :

(i) Registers (ii) Multiplexers (iii) high impedence state (iv) use of control unit (v) Assembly language vi) Micro instrucion format vii) stack viii) Two-address instructions (ix) Indirect address Mode (x) software interrupts. 10x2=20

[Total No. of Questions :9] [Total No. of Printed Pages :4]
(2127)

5501

B.Tech. 3rd Semester Examination

Computer Organisation (CSE/IT)

Paper - IT (ID) - 3001

Time Allowed : 3Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary continuation sheet will be issued.

Note : Attempt **one** question from each section. **Section E** is compulsory.

SECTION - A

1. a) Define Instruction Cycle. Discuss memory reference instruction along with the flowchart. **[10]**

b) Draw the functional block diagram of CPU and memory interface. **[05]**

2. a) Draw & Explain the diagram of 3 to 8 line decoder. **[05]**

b) What is the difference between serial & parallel transfer? Using a shift register with parallel load, explain how to convert serial input data to parallel output. **[10]**

Section - B

3. a) Describe the design of hardwired control unit by sequence counter. **[10]**

b) What are the merits and demerits of using a variable length instruction formats **[05]**

4. Explain Booth's algorithm for multiplication with the help of flow chart. **[15]**

SECTION- C

5. a) Explain the use of stack organization in CPU? How you calculate (a+b) *[c* (d+e)+f] using stack? **[10]**

b) What are the basic differences between branch instruction & call subroutine instruction? **[05]**

6. a) Draw a space-time diagram for a five segment pipeline showing the time it takes to process nine tasks? **[05]**

b) Discuss addressing modes with suitable example? **[10]**

SECTION - D

7. a) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs and outputs? **[10]**

b) Explain the asynchronous data transfer? **[05]**

8. a) An address space is specified by 24 bits & the corresponding memory space b by 16 bits. Find the following: **[3+3+4=10]**

   i. How many words are there in the address space?

   ii. How many words are there in the memory space?

   iii. If a page consists of 2K words, how many pages & blocks are there in the system

   b) Explain the concept of virtual memory? **[05]**

Section - E

9. Attempt all parts:-

   a) What is page fault? **[03]**

   b) Explain write back method in cache memory. **[03]**

   c) What is Microprogram sequencer? **[03]**

   d) What is the use of control memory? **[03]**

   e) What is the maximum speed up that can be achieved by a pipeline. **[03]**

f) What is registers? **[02]**

g) What is use of control unit? **[03]**

h) What is high impedance state? **[03]**

i) Differentiate between RAM and SAM? **[03]**

j) What is page replacement technique. **[03]**

k) What is an Associative memory? **[03]**

l) What is a flipflop. Give the truth table for SR flip flop? **[03]**

m) What is memory hierarchy? **[02]**

n) Define register indirect and relative addressing modes. **[03]**

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Total No. of Questions - 9] Total Pages : 3

(2118)

5920

B.Tech. Third Semester Examination

COMPUTER ORGANISATION

(CSE/IT)

Paper : IT(ID)-3001

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *five* questions in all, selecting *one* each from Sections A, B, C and D. Section E is compulsory.

SECTION–A

1. (a) What is Combinational logic circuit ? How is it different from Sequential logic circuit ? 5

(b) Define Instruction cycle. Discuss memory reference instruction alongwith the flow chart. 10

2. (a) What is a Karnaugh map (K-map) ? Explain its significance. Simplify the Boolean function using K-map.

$F(A, B, C, D) = \Sigma(0, 1, 2, 4, 5, 7, 11, 15)$. 10

(b) How many 128 × 8 memory chips are needed to provide a memory capacity of 4096 × 16 ? 5

SECTION–B

3. (a) Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory ? 10

(b) Define the following :

(i) Micro operation.

(ii) Micro instruction.

(iii) Micro code. 1+2+2=5

4. Draw a flow chart and explain Booth's multiplication algorithm to multiply two signed numbers. 15

SECTION–C

5. (a) What are the basic differences between Branch instruction, Call subroutine instruction and Program interrupt ? 5

(b) Define Interrupt. Give five examples of external interrupts and five examples of internal interrupts. What is the difference between Software interrupt and Subroutine call ? 10

6. What is Pipelining ? Discuss the arithmetic pipeline. 15

2. (a) What are the different types of Interrupts ? Explain the interrupt cycle of computer with the help of a flow chart. 10

(b) What is the significance of using state tables and diagrams for sequential circuits ? Draw the state diagram of a two-bit binary counter with one control signal to start and stop the counter. 10

SECTION–B

3. How addition and subtraction is performed with signed-2's complement data ? Explain the hardware implementation and algorithm. 20

4. What is Control unit ? Explain the working of microprogram sequencer for a control memory in detail. 20

SECTION–C

5. (a) What are the different addressing modes ? Explain the use of each with the help of an example. 10

(b) What are RISC and CISC ? Explain their characteristics. 10

6. How instruction level parallelism is achieved using instruction pipeline ? What are the different conflicts that can occur and how are they resolved ? 20

SECTION–D

7. Discuss Memory hierarchy in a computer system. Also state memory device characteristics. 15

8. What is Cache memory ? Discuss various mapping techniques for transformation of data from main memory to Cache memory. 15

SECTION–E

9. Attempt all parts :

(a) What is a flip-flop ? Give the truth table for JK flip-flop. 3

(b) Name universal gates. Why are they called so ? 3

(c) What is a full adder ? Discuss. 3

(d) Discuss the characteristics of RISC ? 3

(e) What is DMA ? 3

(f) What is Virtual memory ? 2

(g) Differentiate between RAM and SAM ? 3

(h) What is Page replacement technique. 3

(i) Differentiate between Multiplexer and Demultiplexer. 3

(j) Draw the ckt. of MOD 6 counters. 3

(k) What are three address instructions ? 2

(l) What is an Associative memory ? 2

(m) Draw the circuit diagram for Shift register. 2

(n) Define Encoder. 2

(o) Define Addressing mode. State their significance in computers. 3

Total No. of Questions - 9] Total Pages : 4

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B.Tech. IIIrd Semester Examination

COMPUTER ORGANISATION

(CSE/IT)

Paper : IT(ID)-3001

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *five* questions in all, selecting *one* question each from Sections A, B, C & D. Section E is compulsory.

SECTION–A

1. (a) How can you divide the evolution of computers over the years into different generations ? Give the specifications of different components used in each generation. 15

(b) What is the difference between Combinational and Sequential circuits ? Explain the Excitation table for J-K flip-flop. 5

2. (a) What are the different types of Interrupts ? Explain the interrupt cycle of computer with the help of a flow chart. 10

(b) What is the significance of using state tables and diagrams for sequential circuits ? Draw the state diagram of a two-bit binary counter with one control signal to start and stop the counter. 10

SECTION–B

3. How addition and subtraction is performed with signed-2's complement data ? Explain the hardware implementation and algorithm. 20

4. What is Control unit ? Explain the working of microprogram sequencer for a control memory in detail. 20

SECTION–C

5. (a) What are the different addressing modes ? Explain the use of each with the help of an example. 10

(b) What are RISC and CISC ? Explain their characteristics. 10

6. How instruction level parallelism is achieved using instruction pipeline ? What are the different conflicts that can occur and how are they resolved ? 20

SECTION–D

7. (a) What is Priority Interrupt ? Design a Priority encoder. 10

   (b) Explain the process of DMA transfer in computer system. 10

8. (a) Explain the Virtual memory concept. How the logical addresses are mapped with the physical addresses ? 12

   (b) A two way set associative cache memory uses block of four words. The cache can accommodate 1024 words from main memory of size 64 K × 16. Find all the informations required to construct the cache memory. 8

SECTION–E

(Compulsory Question)

9. Attempt all the following : .

   (a) What are the different phases of an instruction cycle ?

   (b) What are the different types of instruction in computer ?

   (c) What is the difference between Microprogram and Microprocessor ?

   (d) What is Control memory ?

   (e) Differentiate between Program interrupt and Subroutine call.

   (f) How many clock cycles are required to process 100 tasks in five segment pipeline ?

   (g) List the different page replacement techniques when page faults occur.

   (h) Draw K-map for $F = \sum m(0, 1, 2, 6)$.

   (i) Differentiate between Write Back and Write Through methods of cache writing.

   (j) List the basic components of Memory management unit. 2×10=20

[Total No. of Questions :5] [Total No. of Printed Pages :2]
(2127)

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B.Tech. 3rd Semester Examination

Object Oriented Methods & Programming (CSE/IT)

Paper - IT (ID) - 3002

Time Allowed : 3Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary continuation sheet will be issued.

Note : Attempt all Questions.

Section - A

I. a) Explain in detail various garbage collection strategies. **[15]**

OR

b) With the help of an example, explain the concept of inheritance in object-oriented programming. **[15]**

Section - B

II. a) Define a class vector. Use overloaded * (multiply) operator to multiply a vector by a scalar. **[15]**

OR

b) With the help of an suitable example, explain the usefulness of function overloading. **[15]**

Section - C

III. a) What is a stream and explain about streams in C++. Write a function template for binary search. **[10+5]**

OR

b) Differentiate between multiple and multilevel inheritance. Class B and class C are derived from a base class A and class D is derived from class B and class C. How a member of class D can have direct access on members of class A. **[5+10]**

Section - D

IV. a) Explain about the basic concepts involved in object - oriented systems design. **[15]**

OR

b) Explain about the basic concepts involved in object - oriented systems analysis. **[15]**

Section - E

V. a) Differentiate between constructor and destructor. **[5]**

b) Define reference variable. Explain about its application with an example. **[5]**

c) Write a note on top - down programing approach. **[5]**

d) Write a note on friend function. **[5]**

e) What are abstract classes? **[5]**

f) Write a note on Entity relationship modelling. **[5]**

g) What is conversion function? How is it created? **[5]**

h) With the help of an example, explain how objects are passed to functions. **[5]**

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Total No. of Questions : 9] Total Pages : 3

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B.Tech. IIIrd Semester Examination

FUNDAMENTALS OF ECONOMICS (IT)

Paper : HU-3001

Time : Three Hours] [Maximum Marks : 100

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/ continuation sheet will be issued.

Note : Attempt *one* question from each section. Section E is compulsory. Section A, B, C & D carry equal marks while Section E carries 40 marks.

SECTION–A

1. Define Demand. Explain the factors that affect demand. 7, 8

2. What is Perfect Competition ? How does a firm achieve its equilibrium in the short and long run under this type of market form ? 5, 10

SECTION–B

3. Define Firm. Explain the objective and types of firm. 5, 10

4. What are the underlying factors which must be taken into account while taking pricing decision ? 15

SECTION–C

5. Analyse the nature of unemployment in advanced and less developed economies. 15

6. What is meant by Trade Cycle ? Describe the various phases of trade cycle. 5, 10

SECTION–D

7. What is meant by the term 'Sustainable Development' ? Explain the role of capital formation in the economic development of a country. 6, 9

8. "British colonialism is also responsible for the economic backwardness of India." Comment upon the statement in the light of India's experience since independence. 15

SECTION–E

(Compulsory Question)

9. Write short notes on the following :

   (a) Exceptions to the Law of demand. (Any *two*)

   (b) Micro Economics and Macro Economics are complementary to each other.

(c) Extension and Contraction in demand.

(d) Alternative pricing policies.

(e) Mergers and Takeovers.

(f) Kinds of Inflation.

(g) W.T.O.

(h) Trends in Economic growth. 5×8=40
